IN THE CLAIMS

Please add claims 13-17 as follows:

13. (New) A data processing system, comprising:

a data processing unit formed on a semiconductor substrate;

a display unit coupled to the data processing unit;

an image input circuit coupled to the data processing unit; and

a synchronous memory coupled to the data processing unit, and provided with a clock signal from the data processing unit,

wherein the data processing unit comprises:

a data processing module accessing to the synchronous memory;

a plurality of registers which includes registers capable of storing an initial set value according to a priority order; and

a control unit controlling arbitration to access to the synchronous memory,

wherein the synchronous memory is accessed by the data processing module, the display unit, and the image input circuit, which modules have a priority order, respectively.

14. (New) The data processing system according to claim 13,

wherein the data processing unit further comprises a plurality of timer units that set the initial set value stored in the registers.

15. (New) The data processing system according to claim 14,

wherein the timer units perform a count-down operation,

wherein one of the timer unit starts the count-down operation, when the control unit receives an access request from one of the modules accessing to the synchronous memory,

wherein the initial set value of a module having high priority order is smaller than the initial set value of a module having low priority order, and

wherein the control unit allows the module, which outputs the access request and relates to the timer unit having the low value, access to the synchronous memory when usable.

16. (New) The data processing system according to claim 14,

wherein each of the data processing module and the display unit have a high priority order, and the image input circuit has a low priority order, and

wherein the initial set value of the high priority order is smaller than the low priority order.

17. (New) The data processing system according to claim 13,

wherein the data processing unit further comprises a memory interface unit operating to access the synchronous memory, and outputting data signals, address signals and control signals, and inputting data signals to the synchronous memory, and

wherein the memory interface unit controls access to the synchronous memory according to arbitration of the control unit.